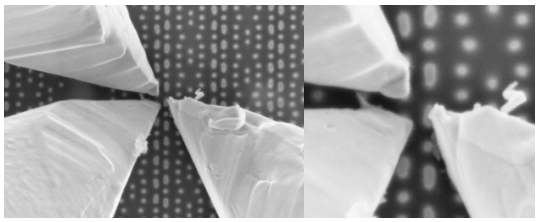
Recent Advances in Electrical Characterization Techniques

Kleindiek Nanotechnik is dedicated to providing you with sophisticated and easy to use tools for performing electrical characterization experiments and in-situ failure analysis with high precision and fast through-put.
This document is intended to give you a brief overview of our recent advances in probing technology.

Probing 32 nm and below

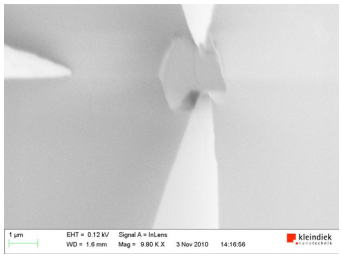


Probing on sub 32 nm device with MM3A-EM probing system

Accessing nano structured semiconductor systems requires highly precise positioning devices as well as perfectly sharpened and conditioned tips. Kleindiek Nanotechnik provides FIB sharpened and cleaned tips with a tip radius of 20 nm.
Another important factor is the quality of the specimen preparation - clean surfaces are necessary for obtaining reliable contacts.

Probing at ultra-low acceleration voltages

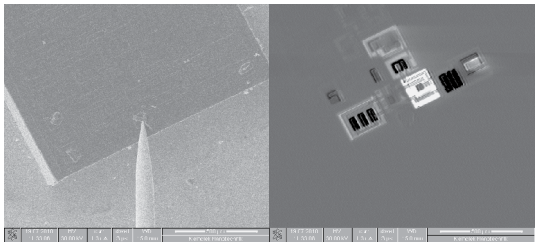
Imaging sensitive structures with an electron beam can induce damage to the sample. Using low acceleration voltages can minimize or prevent damaging the device under test. Using Kleindiek Nanotechnik probers, it is possible to perform electrical characterization experiments at low acceleration voltages.



Probing with 120 V beam voltage at 1.6 mm working distance

EBIC at high frame rates

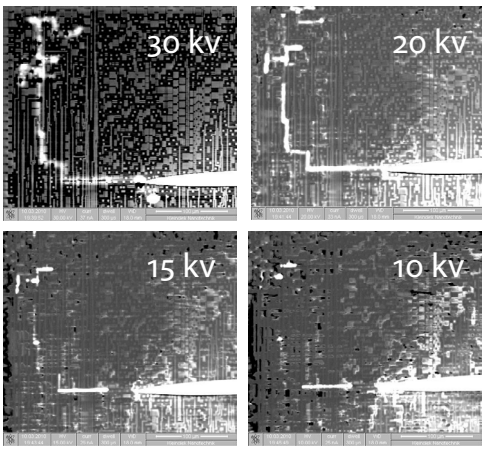
EBIC is a well established method for investigating buried structures in semiconductors. Through great improvements in our EBIC amplifier, we are now able to produce EBIC imagery in real time. Below images depict an operational amplifier shown using the SE-detector (left) and using the EBIC amplifier utilizing a beam dwell time of 3 µs.



SE image (left) and EBIC image (right) taken with a beam dwell time of 3 µs

EBAC / RCI at varying acceleration voltages

Another well established method for investigating buried semiconductor structures is **E**lectron **B**eam **A**bsorbed **C**urrent or **R**esistive **C**ontrast **I**maging. Varying the electron beam's acceleration voltage in consecutive images shows the current response at different depths in the sample.



Failure analysis through 4 metal layers in a CMOS device

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